IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 12, Issue 2, Ver. III (Mar.-Apr. 2017), PP 01-05
www.iosrjournals.org

Implementation of Efficient Johnson Counter Using Diode Free Adiabatic Logic (DFAL)

K. Ram Bharatkumar[1], M. Rajan Babu[2], V. Asha Lakshmi[3], N. Sai Niharika[4]
[1, 2, 3, 4] *(Electronics and communication engineering, Lendi Institute of Engineering and Technology, India)*

Abstract:*This paper describes the implementation of Johnson Counter using different techniques like DFAL, GDI, CPL, 2PASCL, TG, CMOS. For the achievement of low power dissipation mainly DFAL is used. Comparison has shown a significant power saving to the extent of 60% in case of diode free adiabatic logic technique (DFAL). The TANNER EDA tool has been used to stimulate all the circuits. The present research provides a low power ,high speed results up to 100MHZ.and proposal has proved to be used in power aware high performance VLSI circuitry.*

Keywords: *Adiabatic, CMOS, DFAL, CPL, TG, 2PASCL, Energy Recovery, JOHNSON COUNTER, T-SPICE.*

I. Introduction

In the implementation of VLSI design power dissipation makes a major role .In recent years adiabatic system have been used to reduce the power consumption. In this paper we have designed Johnson Counter using different techniques. Among those **DFAL** is more efficient as it reduces power consumption. It stands for a system where a transmission takes place in such a way that no gain or loss of heat or energy occur. The newly achieved adiabatic circuits like **2PASCL, GFAL** mainly endure from large time delay complexity structure.

II. Johnson Counter

A Johnson counter is an also called twisted ring counter. Where the output from the last stage is inverted and fed back as input to first stage. It can be implemented using D-FLIPFLOP or JK-type FLIP FLOP. Here we use D-FLIPFLOP to implement Johnson counter .it can be used in divide the clock inputs by varying their feedback loops. It can also be used in stepper motor controller.

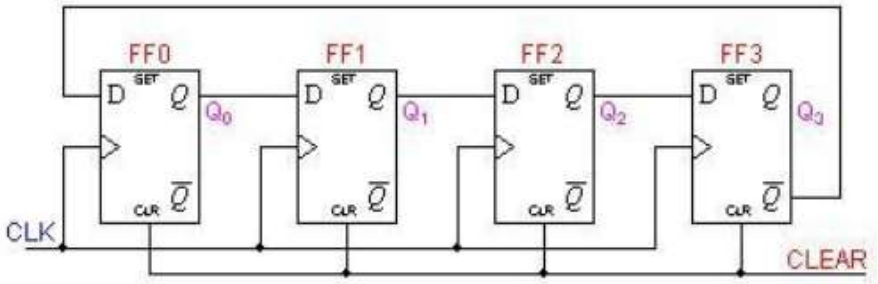

FIG-1

Truth table of Johnson counter is shown in below table.

Clock Pulse No	FFA	FFB	FFC	FFD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

III. D-Flip Flop Using CMOS

Complementary metal-oxide-semiconductor termed as CMOS. It refers to fact that the typical design style in CMOS uses complementary and symmetrical pairs are p-type and n-type semi conductor. CMOS offers high input impedance. It consumes very little power when held in fixed state. CMOS gates are very simple. The basic gate is an inverter. This is only two transistors. This together with the low power consumption means it lends itself well to dense integration or conversely gets a lot of logic for the size, cost and power.

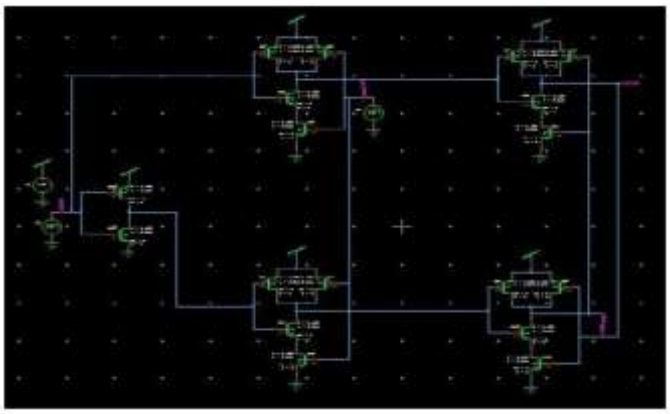

Fig. Schematic Diagram of D-FLIP FLOP (CMOS)

IV. D-Flip Flop Using TG

A TRANSMISSION GATE (TG) is can conduct in both directions or block by a control signal with almost any voltage potential analogous to that of relay. it is CMOS based research passes strong 1,buy poor 0.and NMOS passes strong 0 but poor 1.here transmission gates made up of two field effect transistors.TG is mainly useful for the security application. They can be selectively block critical signals or data from the being transmitted without proper hardware –controlled authorization.

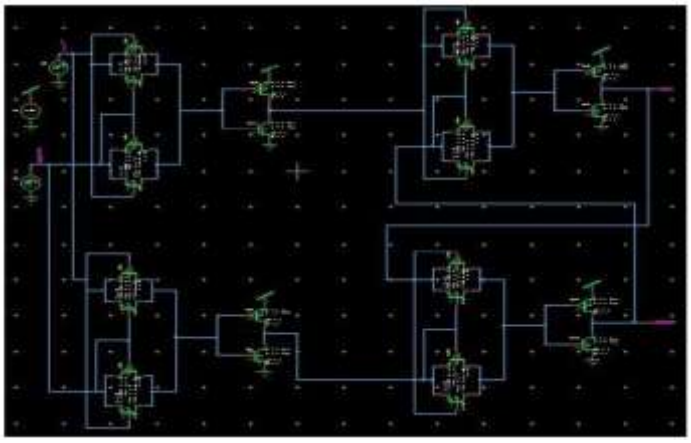

Fig. Schematic Diagram of D-FLIP FLOP (TG)

V. D-Flip Flop Using CPL

The complex logics can be alternatively implemented using CPL (complementary pass transistor logic). CPL is extremely fast and efficient. Some of the examples of CPL circuits are shown in figure.

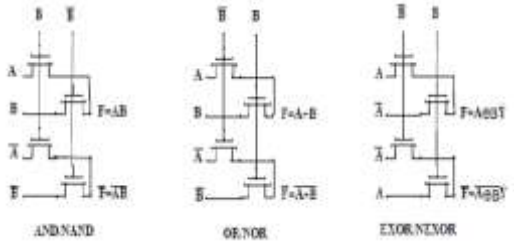

Fig. Realization of Logic Gates using CPL method

CPL is used to reduce the count of transistors used to make different logic gates. Transistors are used as switches to pass logic levels between nodes of circuit. This reduces the number of active devices. CPL makes designing of gates is simpler. CPL design is modular .All gates follow same topology.CPL design is modular All gates follow same topology. CPL the logic voltage levels of sequential chain do not decrease.

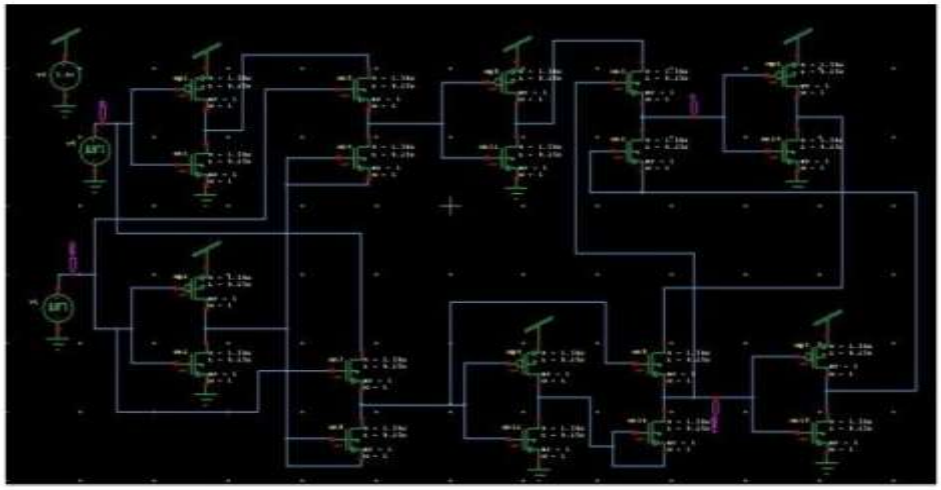

Fig. Schematic Diagram of D-Flip Flop (CPL)

VI. D-Flip Flop Using GDI

GDI (GATE DIFFUSION INPUT) is a new technique for low power digital combinational circuit. This technique allows reduce in power consumption, propagation delay and area of digital circuits. While maintaining low complexity of logic design .GDI cell contains three inputs. They are G(common gate input of NMOS and PMOS), P(input to the source/drain of PMOS) and N(input to the source/drain of NMOS).

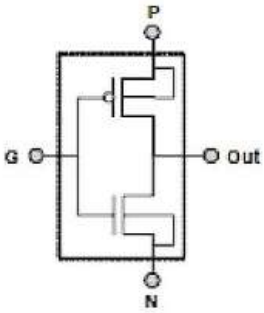

Fig.GDI cell

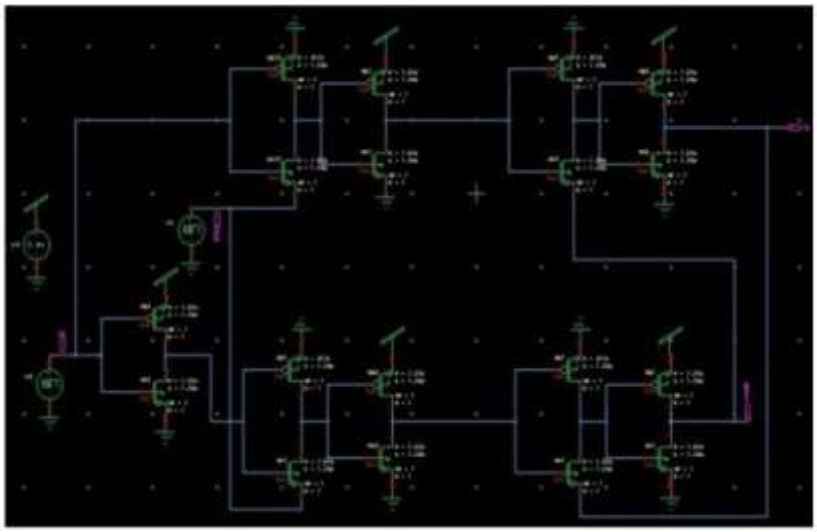

Fig. Schematic Diagram of D-Flip Flop (GDI)

VII. D-Flip Flop Using 2PSAL

In this technique we use the phase shift adiabatic logic. We have undergone less delay ad high switching speed. In this 2PSAL output amplitude is very less. And main advantage of this circuit is having the least power consumption too.

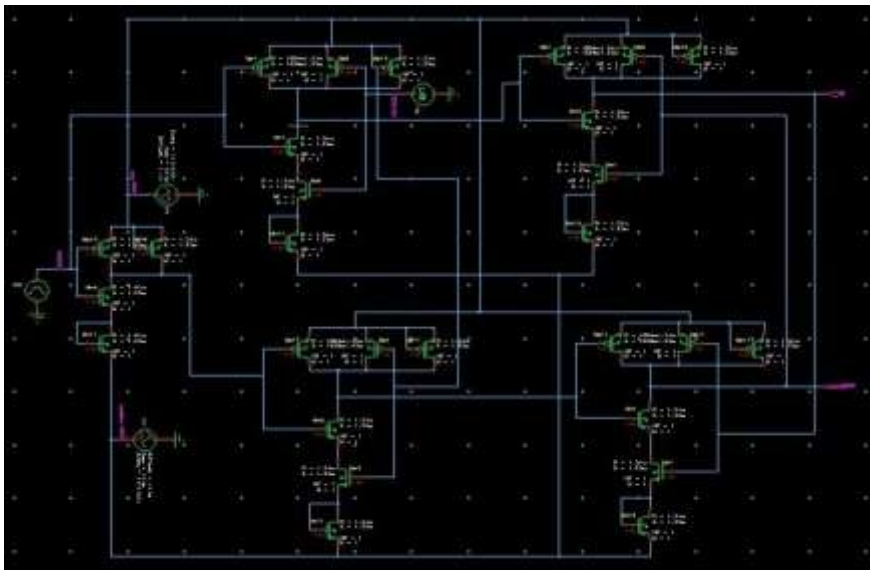

Fig. Schematic Diagram of D-Flip Flop (2PSAL)

VIII. D-Flip Flop Using DFAL

The adiabatic logic achieves the task of low power consumption. And achieves higher circuiting speed. With the using of DFAL there is saving of 60% of energy when compared to all techniques circuits .this shows less time delay. DFAL requires less number of transistors for circuit operation. With the using of DFAL we can construct circuit like full adders, full sub-tractors.

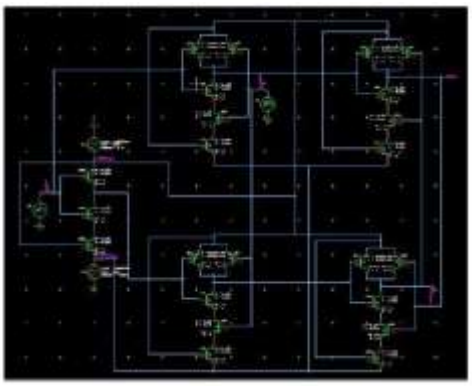

Fig. Schematic Diagram of D-FLIP FLOP (DFAL) **Fig.** Output Wave forms of the DFAL Technique

IX. Johnson Counter Using DFAL

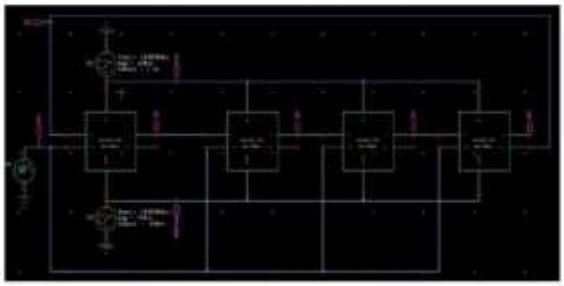

Fig. Schematic Diagram of Johnson counter (DFAL) **Fig.** Output Wave forms of the DFAL Technique *Paper*

X. Conclusion

This paper concluded that by comparing johnson counter with all other techniques like GDI,TG,CPL,2PSAL,CMOS,DFAL.we attain less power consumption of DFAL when compared with other techniques.where high circuit speed achieved and higher output amplitude is achieved.the stimulation results and comparitive performance evaluation revealed that power consumption and over all pdp DFAL is best one.

XI. Comparison of Different Johnson Counter Techniques

We have designed Johnson counter in different techniques. Each technique has its own advantages and disadvantages. Below table shows the comparison of all these techniques.

Technology	Average power	Peak power	Delay	Pdp
CMOS	9.6123m	55.7542m	8.8824n	0.495231n
TG	32.6120m	1222.8003m	334.7523p	0.07457689n
CPL	67.5790m	209.5852m	6.4409n	1.349917315n
GDI	19.9996m	37.9022m	54.5414n	2.0672n
2PSAL	135.6613m	533.7345m	4.9614n	2.6480n
DFAL	10.4409m	20.3375m	35.8237n	0.035646237n

Table: Power Dissipation comparison of DFAL with different techniques

References

Journal Papers:

[1]. Shipra upadhya R.A Mishra, Nagari,and SP Singh, Diodefreeadiabaticlogiccircuits, hindawan ipublished corporations ISRN Electronics Volume 2013, Article ID 673601.

[2]. Atul Kumar Maury & Gagnesh Kumar, Energy Efficient Adiabatic Logic for Low Power VLSI Applications, 2011 International Conference on Communication Systems and Network Technologies.

[3]. N. Waste and K. Eshraghian, Principle of CMOS VLSI Design: A System Prospective, 2nd New York: Addison – Wesley, 1993.

[4]. W. C. Athas, L. J Svensson, J. G. Koller, "Low- power digital systems based on adiabatic, switching principles" IEEE Trans. On VLSI systems, 2(4), Dec. 1994, pp: 398-407.

[5]. Prasad D Khandekar, Dr.Mrs Shaila Subbaraman, Low Power 2:1 MUX for Barrel Shifter, First International Conference on Emerging Trends in Engineering and Technology.

[6]. Abhijit Asati & Chandrasekhar VLSI Implementation of a High Performance Barrel Shifter Architecture using Three Different Logic Design Styles, International Journal of Recent Trends in Engineering, Vol 2, No. 7, November 2009.

[7]. Shweta Chawla, Raman and Harijan, Harpal singh, Design Low Power 32-Bit Barrel shifter using Efficient Charge Recovery Logic. International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-2, Issue-3, February 2013.

[8]. Arun kumar Manoj Sharma, design and analysis of mux using adiabatic techniques ECRL AND PFAL, 978-1-4673-6217-7/13/$31.00_c 2013 IEEE

[9]. Gate-diffusion input (gdi) - a technique for low power design of digital circuits: analysis and characterization Arkadiy Morgenshtein', Alexander Fish2 and Israel A. Wagner'